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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,634	11/26/2003	Daniel Mulligan	SIG000110	9718
34399	7590	04/04/2005	EXAMINER	
GARLICK HARRISON & MARKISON LLP			TRAN, ANH Q	
P.O. BOX 160727			ART UNIT	PAPER NUMBER
AUSTIN, TX 78716-0727			2819	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/723,634	MULLIGAN, DANIEL
	Examiner Anh Q. Tran	Art Unit 2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 26 November 2003.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) 9-15 is/are allowed.

6) Claim(s) 1,4,5,8,16-19 and 23 is/are rejected.

7) Claim(s) 2,3,6,7 and 20-22 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_

5) Notice of Informal Patent Application (PTO-152)  
6) Other: \_\_\_\_\_

**DETAILED ACTION*****Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 are rejected under 35 U.S.C. 102(e) as being anticipated by Klapproth (6,580,288).

Klapproth shows:

1. A configurable integrated circuit comprises: at least one general purpose input/output (GPIO) interface module (260 or 270, Fig. 2) that includes a plurality of GPIO cells, wherein a GPIO cell (315, Fig. 3) of the plurality of GPIO cells is operably coupled to a corresponding pin (305) of the configurable integrated circuit, wherein, when the configurable integrated circuit is in a first functional mode (high signal input to control pin 355, col. 5, lines 15-19), the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital input pin and when the configurable integrated circuit is in a second functional mode (low signal input to control pin 355, col. 5, lines 26-30), the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital output pin;

a first functional module (360) having a connection operably coupled to the GPIO cell when the configurable integrated circuit is in the first functional mode; and second functional module (365) having a connection operably coupled to the GPIO cell when the configurable integrated circuit is in the second functional state.

4. The configurable integrated circuit of claim 1, wherein the first function module and second function module comprises at least one of: a random access memory (RAM) interface module (address circuit are associated with RAM).

5. The configurable integrated circuit of claim 1, wherein each of the plurality of GPIO cells comprises: a data input buffer (triangle shape between 305 and 345) having an input and an output, wherein the input of the data input buffer is operably coupled to the corresponding pin;

    a data output buffer (triangle shape between 305 and 325) having an input and an output, wherein the output of the data output buffer is operably coupled to the corresponding pin;

    a data input connection operably coupled to, when enabled, provide an inbound data signal from the output of the data input buffer to the first functional module (360); a data input register (345) operably coupled to, when enabled, store the inbound data signal for subsequent access by a processing core;

    a data output connection operably coupled to, when enabled, provide an outbound data signal from the second functional module (365) to the input of the data output buffer; a data output register (325) operably coupled to, when

enabled, provide an alternate outbound data signal to the input of the data output buffer; and

an input/output selection module (170, Fig. 1) operably coupled to enable at least one of the data input buffer, the data output buffer, the data input connection, the data input register, the data output connection, and the data output register.

8. The configurable integrated circuit of claim 1, wherein the at least one general purpose input/output (GPIO) interface module further comprises:

a first GPIO interface module operably coupled to the first and second functional;

a second GPIO interface module operably coupled to a third functional module and a fourth functional module (col. 4, lines 31-49), wherein, when the configurable integrated circuit is in a third functional mode, a GPIO cell of the second GPIO interface module is operably coupled to a second corresponding pin such that the second corresponding pin functions as a digital input pin and when the configurable integrated circuit is in a second functional mode, the GPIO cell of the second GPIO interface module is operably coupled to the second corresponding pin such that the second corresponding pin functions as a digital output pin.

#### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ziklik et al (5,402,14).

Ziklik shows a multiple function system (Fig. 3) comprises:

a processing module (301); on-chip memory (307) operably coupled to the processing module; memory interface (312A-C, col. 5, lines 19-21) for accessing off-chip memory, wherein at least of the on-chip memory and the off-chip memory store operational instructions that cause the processing module to perform at least one of a data file storage function; a plurality of functional modules (355-357) operably coupled to the processing module, and at least one general purpose input/output (GPIO) interface module (304A) operably coupled to the plurality of functional modules and the processing module, wherein the at least one GPIO includes a plurality of GPIO cells (col. 6, lines 3-4), wherein a GPIO cell of the plurality of GPIO cells is operably coupled to a corresponding pin (400, Fig. 4) of the multiple function system of a chip integrated circuit, wherein, when the multiple function system is in a first functional mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital input pin and when the multiple function system of a chip integrated circuit is in a second functional mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital output pin (col. 7 & 8).

Ziklik discloses the claimed invention except for integrating a processing module and a plurality of functional modules on a chip. It would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate a processing module and a plurality of functional modules of Ziklik on a chip, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together on a chip involves only routine skill in the art.

17. The multiple function system on a chip integrated circuit of claim 16 further comprises:

programmable logic fabric (311A- E, col. 6, lines 17-20) operably coupled between the at least one of GPIO interface and at least one of the plurality of function modules.

18. The multiple function system on a chip integrated comprises'. circuit of claim 17 further remaining GPIO cells of the plurality of GPIO cells are operably coupled to the programmable logic fabric, wherein the programmable logic fabric is programmed to provide at least one of:

coupling between at least some of the remaining GPIO cells and corresponding pins of a set of pins of the configurable integrated circuit; processing of inbound digital signals when the multiple function system of a chip integrated circuit is in the first functional mode; and processing of outbound digital signals when the multiple function system of a chip integrated circuit is in the second functional mode (col. 7-8).

19. The multiple function system on a chip integrated circuit of claim 16, wherein the plurality of function modules two or more of: random access memory module.

23. The multiple function system on a chip integrated circuit of claim 16, wherein the at least one general purpose input/output (GPIO) interface module further comprises: a first GPIO interface module (304A) operably coupled to first (355) and second (356) functional modules of the plurality of functional modules; and a second GPIO interface module (304B) operably coupled to a third (357) and fourth functional modules (306) of the plurality of functional modules, wherein, when the configurable integrated circuit is in a third functional mode, a GPIO cell of the second GPIO interface module is operably coupled to a second corresponding pin such that the second corresponding pin functions as a digital input pin and when the configurable integrated circuit is in a second functional mode, the GPIO cell of the second GPIO interface module is operably coupled to the second corresponding pin such that the second corresponding pin functions as a digital output pin (304A and 304B connected to all the function modules by 311A-E).

***Allowable Subject Matter***

5. Claims 2-3, 6-7, 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 9-15 are allowed.

7. The following is an examiner's statement of reasons for allowance: the connection of pins, circuits, and register responsive when mode selection signal in first to fourth state as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN  
PRIMARY EXAMINER

  
3/31/05